Electrical Characterization of Serial ATA Interconnection at Gigabit Speeds

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SCOPE

- Serial ATA Technology Overview
- Characterization of Serial ATA Cable Interconnection
- Modeling, Simulation and Validation of Serial ATA Cable
- Conclusion
What is Serial ATA (SATA)?

- Next Generation Internal Storage Interconnect
- Point-to-Point, High Speed Serial Interface (150 Mbytes/sec)
- Thinner, longer cables for easier PCB routing
- Low signal Pin count requires less board space
- Low Voltage Differential Signaling with 8b/10b encoding
- Hot-Swap Capability
- 100% Software Compatible “Drop-in” replacement for current ATA
- Visit [www.serialata.org](http://www.serialata.org) for more information.

Parallel Ultra ATA vs. Serial ATA

<table>
<thead>
<tr>
<th>Key Technology</th>
<th>Ultra ATA</th>
<th>Serial ATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Data Rate</td>
<td>100 – 133 Mbytes/sec</td>
<td>150 Mbytes/sec</td>
</tr>
<tr>
<td>Bus Architecture</td>
<td>Parallel</td>
<td>Serial</td>
</tr>
<tr>
<td>Bus Connection</td>
<td>Master/Slave Shared Bus</td>
<td>Point to Point Dedicated Bus</td>
</tr>
<tr>
<td>Clock Strategy</td>
<td>Non-interlocked</td>
<td>Embedded</td>
</tr>
<tr>
<td>Cabling</td>
<td>80-wire ribbon cable</td>
<td>4-wire cable with shield/drain wires</td>
</tr>
<tr>
<td>Connectors (Signal Pins)</td>
<td>80 signal pins</td>
<td>4 signal pins</td>
</tr>
<tr>
<td>PCB Routing</td>
<td>Parallel Data &amp; Clock Routing</td>
<td>Differential Pair Routing</td>
</tr>
<tr>
<td>Signaling</td>
<td>Legacy 5V</td>
<td>LVDS</td>
</tr>
<tr>
<td>Hot-Plug</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Bandwidth Scalability</td>
<td>No</td>
<td>6 Gb/s</td>
</tr>
</tbody>
</table>
Data Storage Interface Speed Roadmap

Serial ATA Physical Interface – Cable Link

<table>
<thead>
<tr>
<th>Approximate Data Rates (10b Speed)</th>
<th>Generation 1</th>
<th>Generation 2</th>
<th>Generation 3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1.5 Gb/s</td>
<td>3.0 Gb/s</td>
<td>6.0 Gb/s</td>
</tr>
</tbody>
</table>

Source: Serial ATA Industry Specification 1.0, Aug 2002
Serial ATA High Speed Performance Targets

<table>
<thead>
<tr>
<th>High Speed Parameter</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mated Connector Impedance</td>
<td>100 Ohms +/- 15%</td>
</tr>
<tr>
<td>Cable Absolute Impedance</td>
<td>100 Ohms +/- 10%</td>
</tr>
<tr>
<td>Cable Pair Matching</td>
<td>+/- 5 Ohms</td>
</tr>
<tr>
<td>Common Mode Impedance</td>
<td>27 ~ 40 Ohms</td>
</tr>
<tr>
<td>Insertion Loss</td>
<td>6 dB max.</td>
</tr>
<tr>
<td>Near-End Crosstalk (NEXT)</td>
<td>-26 dB</td>
</tr>
<tr>
<td>Rise time</td>
<td>85ps max</td>
</tr>
<tr>
<td>Inter-Symbol Interference</td>
<td>50ps max</td>
</tr>
</tbody>
</table>

Note: Requirements applicable to Generation 2 speed.

Serial ATA Cable Assembly Design

- Signal Cable
  - Amphenol Spectra-Strip SkewClear 26 AWG Cable
  - 2 differential signal lines with grounds
  - Differential 100 Ohms
  - Point to point unidirectional construction
  - Generation 1 & 2 Performance levels
  - Can customize for any length under 1 meter
  - Small flexible cable for easy routing and no airflow restriction

- Cable Receptacles
  - Passive latching detent, vibration resistance
  - Low mating force
  - Positive polarization with visual indicator

Gen 2 High Speed Cable Device Plug
Serial ATA Cable Assembly Characterization

- High Speed Test Vehicle
  - Test Fixture Board
    - Controlled Impedance Signal Traces
    - Field Replaceable SMA interface
    - Calibration test structures
  - Test Methods
    - EIA-364 Electronics Test Methods
    - Test conditions as specified in Serial ATA 1.0 Performance Specification
  - Test Parameters
    - Differential/Common Mode TDR Impedance
    - Rise Time Degradation
    - Delay Skew
    - Insertion Loss
    - Near-End Crosstalk
    - Eye Pattern
  - Test Equipment
    - High Speed Digital Sampling Oscilloscope with DTDR
    - High Speed Pulse Pattern Generator
  - Modeling Software
    - TDA Systems IConnect Software

- High Speed Measurement Setup

Differential Impedance Measurement
TDR Launch Rise Time

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**SMA**

**PCB Trace**

**Input of Device Plug**

**Short-circuited**
Differential Impedance Measurements
Mated Connector & Cable Media Impedance

Mated Connector
Raw Cable

TDR Risetime = 40ps

Differential Impedance Measurements
Mated Connector Impedance

TDR Risetime = 40ps
Differential Impedance Measurements
Cable Match Performance at Generation 2

TDR Risetime = 70ps

Common Mode Impedance Measurements
Generations 1, 2 and 3
**Differential and Common Mode Impedance**

- Generation 3
  - Differential Impedance
  - Common mode Impedance
- Generation 2
  - Differential Impedance
  - Common mode Impedance

**Intra-Pair Skew Measurements**

- Pair A Delay Skew: 18 ps intra-pair skew
- Pair B Delay Skew
Differential Insertion Loss (S21)

Eye Pattern Measurements
K28.5 Data Pattern, < 30ps, Vin=800mV

Generation 1
1.5Gb/s

Generation 2
3.0Gb/s

Generation 3
6.0Gb/s

System Calibration: Fixture Without Cable Assembly

1.5Gb/s
3.0Gb/s
6.0Gb/s

Fixture with Serial ATA Cable Assembly
TDA Systems, Inc. IConnect® Software

- Measure board **impedance** and **propagation delay**
  - Analyze failures, resolve smaller discontinuities
- Predict **eye diagram degradation** using lossy line model and eye-diagram display
- Model **crosstalk** and **jitter** in a differential coupled line
- Model reflections and ringing in a trace on a PCB, including connectors, cables, sockets, packages
- Validate models from field solver using IConnect integrated interface to SPICE simulators
- Analyze losses and resonances using **S-parameter computation**
- Obtain package or connector parasitic

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TDA Systems, Inc. IConnect® Software

- SPICE / IBIS Simulation (HSpice, PSpice, BSpice)
- Field Solver Analysis
- Accurate validated models for interconnects

- TDR Measurement
- Agilent, Tektronix TDR

- Correlate SPICE simulation to TDR measurement
Serial ATA Cable Assembly Modeling Strategy using IConnect®

- Mated Connector Modeling
  - Full Coupled Line Model
  - Differential/Common Mode TDR Measurement
  - Odd/Even Mode Responses
  - Predict Connector/Cable Impedances

- Cable Assembly Modeling
  - Lossy Line Model
  - Differential TDR/TDT Measurement
  - Predict Eye Diagram and Insertion Loss (S21)

- Composite Model Generation and Simulation

- Model Verification and Validation

**Full Coupled Line Connector Model Extraction**

[SPICE Netlist]

* Time Domain Analysis Systems: IConnect
  .subckt Connector_Model port1 port2 port3 port4 gnd_
  Partition #1
  t1 port1 gnd_ 1 gnd_Z0=92 TD=53.4p
t2 port3 gnd_ 2 gnd_Z0=92 TD=53.4p
t3 port1 port3 1 2 Z0=318 TD=53.4p
  Partition #2
  t4 1 3 4 5 Z0=44.3 TD=41.9p
t5 2 3 6 5 Z0=44.3 TD=41.9p
t6 3 7 8 2
e1 9 5 9 10 2
t7 7 6 10 Z0=22.1 TD=41.9p
t8 8 gnd_ 10 gnd_Z0=68.9 TD=80p
  Partition #3
  t9 4 gnd_ port2 gnd_ 62.3 TD=111p
t10 6 gnd_ port4 gnd_ 62.3 TD=111p
t11 4 6 port2 port4 Z0=398 TD=111p
.ends

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**Serial ATA Signal Pinout**

- G
- B+
- B-
- G-
- A-
- A+
- G
Simulate and Validate Models
Odd and Even Mode Responses

Odd-Mode Model Correlation

Cable Lossy Line Modeling

Lossy Line SPICE Netlist

Odd-Mode Model Correlation
Composite Model Generation

Model Validation
Predicted and Measured Eye Diagrams

1.5Gb/s (Gen 1)

3.0Gb/s (Gen 2)

6.0Gb/s (Gen 3)
Summary

- Characterization of Serial ATA Cable for Generations 1, 2 and 3 speeds.
- Conformance of Serial ATA Cable link capable up to Generation 2 speeds.
- Usage of TDA Iconnect Modeling software to extract, model and validate accurate SPICE models of the cable assembly.

For more information on Serial ATA Solutions, visit Molex at Booth 427.