Application Note

# Measurement of Input and Output Die Capacitance for M-LVDS and Other Signaling Standards Using TDR

## Measurement Technique

Input capacitance of the buffer will affect the overall signal integrity of the digital circuit, and knowing this capacitance is important to understand the circuit performance. In many fast signaling standards, such knowledge is mandated by a given standard. For example, a new ANSI/TIA/EIA-899 M-LVDS standard [1] requires the designer to test for both input capacitance to ground (single-ended capacitance, $C_1$, $C_2$ in Figure 1) and capacitance between the differential line pair (differential capacitance $C_{12}$ in Figure 1).

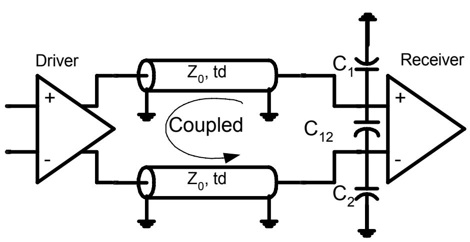


**Figure 1. Test of single-ended and differential input capacitance of the driver is often required by the signaling standards.**

The same techniques used by IC package designers to measure package capacitance can be applied for measuring the combined input buffer and package capacitance. These techniques utilize Time Domain Reflectometry (TDR) oscilloscopes, and the procedure for input package capacitance measurement has been standardized by the JEDEC packaging committee [2], further reported in [3], and implemented in TDA Systems' IConnect® TDR software. This input capacitance measurement is a relative measurement, comparing the reference open waveform (at the end of the probe or fixture) to the waveform reflected from the capacitive device under test (DUT). This relative measurement allows the designer to easily de-embed the probe or fixture from the measurement. The difference between the reference and the reflected waveform is caused by the capacitance of the DUT, Figure 2.

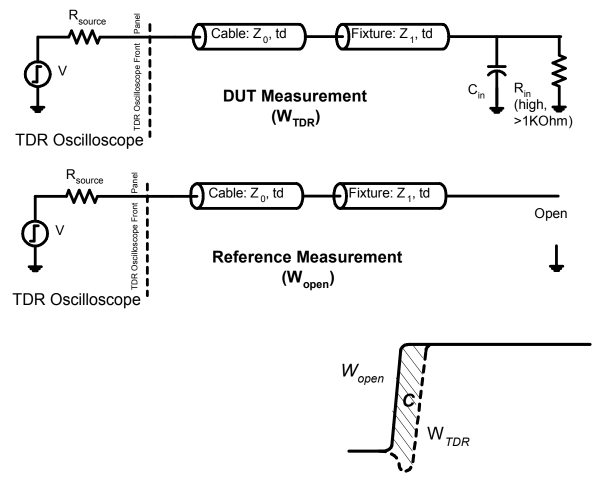


**Figure 2. Self-capacitance measurement.**

The easiest way to perform a measurement is to socket the packaged IC device on a test fixture board, with traces on the board leading to the device pins that need to be tested, and with SMA connectors mounted on the board and connected to these traces. A customer demonstration board for this device, or an ATE fixture board will work well. By using this configuration, the designer can easily connect the test fixture to the TDR oscilloscope, and the socket allows the designer to obtain a reference waveform (empty test board, not DUT in the socket) and the DUT waveform (packaged device placed in the socket) without the difficulty of soldering and de-soldering the DUT.

If placing the DUT in the socket is not a viable option, then having a second fixture board, fully identical to the one on which the DUT is mounted, but without the DUT in place, should provide a good quality reference waveform. One can also use a probe in order to take the measurements, but since TDR measurement always requires a signal and a ground connection [4], a ground pin must be available next to the pin under test, and the pitch of the probe must match the device pitch.

An input buffer will have an input resistance along with the capacitance. There may also be off-chip termination resistors or ESD structures that may affect the capacitance measurement. The input resistance of a CMOS buffer is higher than 1kOhm, it can effectively be treated as an open, ensuring that the measurement is performed correctly. However, the designer has to remove any off-chip termination resistors and ESD diodes in order to accurately obtain the input buffer capacitance.

Since $C_{in}$ changes with changes of the power level applied to the die, it is important to perform a sweep of input capacitance measurements vs. power supply voltage. When performing a TDR measurement with the device in power-up state, one concern is that the DC power from the die can be injected into the TDR line, and thus damage the TDR sampling head input, or at least confuse the measurement results. However, for high-input impedance CMOS gate, this is not really an issue, since very little current flows through the gate of the CMOS driver. The power voltage therefore does not enter the TDR line and does not create any problems with the measurement.

In all of these cases, we effectively are measuring combined package capacitance $C_{package}$ and die input capacitance $C_{die}$, which is what is required by the M-LVDS standard. If it is desired to separate $C_{package}$ from $C_{die}$, the designer needs to have an empty package sample. Then, measuring this empty package sample, the designer can measure $C_{package}$, and $C_{die}$ can then be found as: $C_{die} = C_{buffer} - C_{package}$.

The JEDEC input buffer capacitance measurement procedure described above works well for characterizing capacitance values that generate waveforms similar to those shown on Figure 2 above. In case of input or output buffer capacitance, sometimes the internal reflections at stubs and T-junctions inside the buffer can create the TDR waveforms that look more like the one shown in Figure 3.

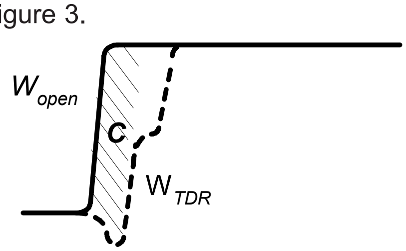


**Figure 3. Capacitance waveforms in presence of the internal stubs and reflections inside the buffer.**

In a case like the one shown in Figure 3, a more accurate capacitance value can be obtained by computing it from the true impedance profile (Z-line) computed in IConnect [4]. This true impedance profile can be easily computed using the same $W_{TDR}$ waveform as the DUT waveform and $W_{open}$ as the reference open waveforms. Once the true impedance profile is computed, all the multiple reflections are de-convolved, and the stub related reflections could be windowed out. The resulting capacitance cursor readout in IConnect gives a more accurate buffer capacitance value.

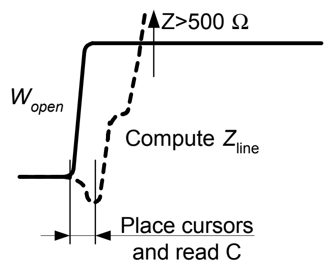


**Figure 4. Computing input capacitance from the true impedance profile in IConnect TDR software.**

Note that even though measuring the capacitance using other measurement techniques, such as LCR meter, will provide a better correlation with the TDR capacitance measurement JEDEC standard procedure (provided the designer can ensure a direct contact between the LCR meter probe and the DUT), the impedance profile based computation will give a more accurate number. In addition, in a case where the die buffer includes a series or parallel termination, the true impedance profile approach is the only valid computational procedure.

Differential input buffer capacitance is measured the same way that the single-ended input buffer capacitance is measured, except the differential stimulus must be applied to the DUT.

## Measurement setup and results

In this example, the packaged device was placed in a socket on the board, and an SMA coaxial cable launch was used to connect the board to the TDR oscilloscope. In order to perform the measurement, the DUT board must have a chassis ground that is isolated from the DUT ground ($V_{ss}$). The designer AC-coupled the chassis ground and $V_{ss}$ together at the perimeter of the board and at each of the local power pin decoupling locations. It was then possible to force an offset voltage between the chassis ground and DUT ground, without injecting additional DC voltage into the TDR head.

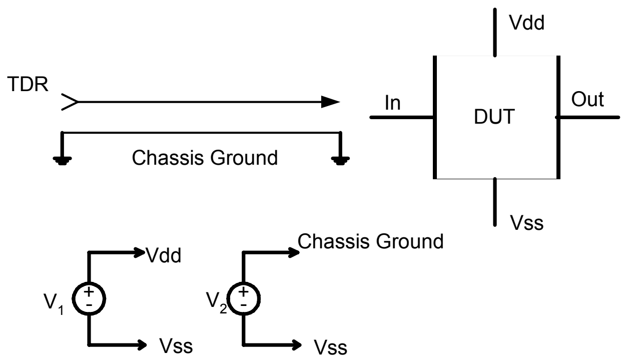


**Figure 5. Measurement set up of chassis ground in reference to DUT ground. Since the power supplies float relative to the chassis ground, changing $V_2$ allows us to vary the TDR offset voltage to DUT $V_{ss}$.**

A typical DUT TDR waveform and a reference open waveform are shown in Figure 6 below. These data are acquired from the TDR oscilloscope and the resulting capacitance is computed in IConnect TDR software.

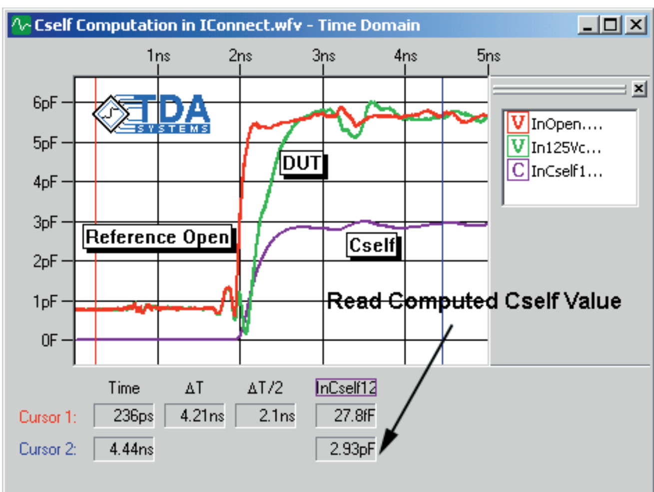


**Figure 6. Computing and reading Cself value in IConnect TDR software.**

Note that the reading is done when the $C_{self}$ waveform reaches its steady state value, as prescribed in [2], [3]. To ensure that it is possible for the waveform to reach its steady state value, the designer must capture a TDR window that is long enough to ensure that the DUT and the reference open waveforms converge together and reach the same voltage level. If there is DC offset between the DUT and the reference open waveform, then a difference between cursor 2 and cursor 1 must be read. If this DC offset is due to the oscilloscope-related factors, then re-calibrating the oscilloscope would typically remove the offset. However, DC offset may also occur if the external termination resistors or ESD diodes have not been removed from the DUT package.

Figure 7 shows the plot of input buffer capacitance measured using the technique described above vs. the input voltage at the buffer $V_{cm}$, where $V_{cm}$ is the sum of the TDR voltage at the DUT[1] and the voltage $V_2$.

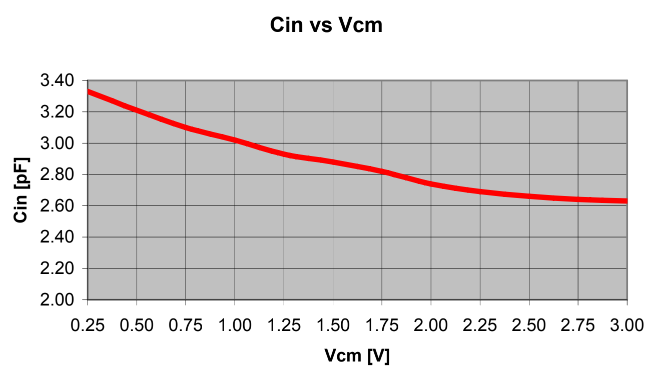


**Figure 7. Input buffer capacitance vs. input voltage at the DUT.**

One quickly notices that the DUT waveform shown in Figure 6 looks very much like the DUT waveform shown in Figure 3. Therefore, we should consider using the impedance profile approach for this type of data. When applying the impedance profile approach, we obtain a smaller and more accurate value of 1.8pF for the input buffer capacitance, Figure 8. Note the placement of cursors at the beginning (red cursor) and the end (blue cursor) of the capacitive buffer. The corresponding capacitive values given in Figure 7 must be re-computed for each voltage level.

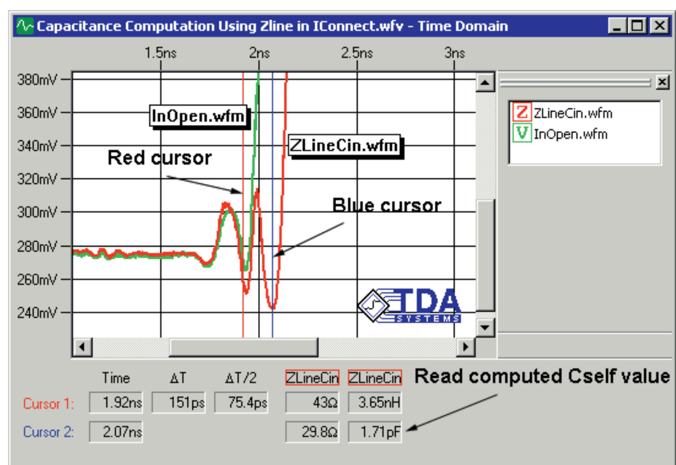


**Figure 8. Reading the capacitance value from the true impedance profile computed in IConnect. Note the placement of cursors.**

[1]Note that only half of the initial TDR voltage actually reaches the DUT; if your instrument initial voltage is 0.5V, you will observe 0.25V at the DUT, if your instrument initial voltage is 0.4V, you will observe 0.2V at the DUT.

For ***output capacitance measurement***, an output DUT pin, instead of the input DUT pin, must be tested.

For ***differential capacitance measurement***, the designer needs to switch the TDR oscilloscope in differential mode, and perform all the above measurements differentially. To remove the potential asymmetry in the board or package traces when measuring differential capacitance, or asymmetry in the capacitances of the buffer, it is best to obtain two DUT waveforms (positive switching channel, $W_{dut\ positive}$, and negative switching channel, $W_{dut\ negative}$,) and two reference open waveforms ($W_{open\ positive}$ and $W_{open\ negative}$), subtract the negative switching channel from the positive switching channel ($W_{dut} = W_{dut\ positive} - W_{dut\ negative}$ and $W_{open} = W_{open\ positive} - W_{open\ negative}$), and then use $W_{dut}$ and $W_{open}$ to compute the buffer capacitance. One should expect that since the differential capacitance of the buffer can be roughly viewed as the capacitances of the two buffers in series, the total capacitance will be approximately half the capacitance of in the single-ended measurement. It is also worth noting that it is not possible to vary the input voltage at the differential buffer using the technique described above for the single-ended capacitance, since the differential input voltage is defined by the difference between the TDR voltages on the positive and negative channels and is not referenced to the DUT ground.

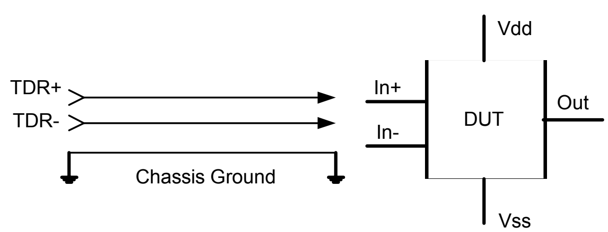


**Figure 9. Differential capacitance measurement.**

## Bibliography

[1] Electrical Characteristics of Multipoint-Low-Voltage-Differential-Signaling, – ANSI/TIA/EIA-899 standard

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[3] D. Smolyansky, "TDR Techniques for Characterization and Modeling of Electronic Packaging," – High Density Interconnect Magazine, March-April 2001, TDA Systems Application Note PKGM-0101

[4] D. Smolyansky, "TDR primer," – PCB Design Magazine, April 2002, TDA Systems Application Note TDR1-0302


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